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Remarks/Arguments

Claims 1, 3-6, 8 and 9 are pending. Claims 1 and 6 stand finally rejected under 35 U.S.C. 103(a) as being unpatentable over Swenson (United States Patent No. 5,926,120) in view of Zaun (United States Patent Publication No. 2002/0024610). Claims 3, 4, 5, 8 and 9 stand finally rejected under 35 U.S.C. 103(a) as being unpatentable over Swenson in view of Zaun, and further in view of Pannell (United States Patent No. 6,636,483). Applicant traverses these rejections for at least the following reasons.

To establish a *prima facie* case of obviousness, all of the recited claim limitations must be taught or suggested in the prior art. *See, MPEP 2143.03; see also, In re. Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).* The cited art fails to teach or suggest each of the limitations of pending Claims 1, 3-6, 8 and 9 for at least the following reasons.

Summary of the Claimed Invention

The present invention provides a serial compressed bus interface, wherein received serial data is converted to packets of parallel data, and the packets of parallel data are transferred to an appropriate one of a plurality of devices associated with data applications in response to a signal from an enable logic.

In the exemplary embodiment, the serial data is received and converted to parallel data by serial to parallel converter 110. The parallel data is transferred to one of the buffers 130-136 in response to the buf_sel signal from enable logic 112. That is, the output of the enable logic 112 identifies which one of the buffers 130-136 is associated with a particular packet of parallel data output from serial to parallel converter 110. Such an arrangement advantageously reduces the pin count required in a serial interface, which receives time-division multiplexed serial data from a plurality of data sources and must transfer each respective data packet to an appropriate data application.

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Claim 1 broadly encompasses the above by reciting:

a serial-to-parallel converter having a single serial data input line adapted to receive time-division multiplexed serial data from a plurality of data sources, and having a plurality of parallel output lines for providing thereon a packet of said time-division multiplexed serial data in parallel form to one of a plurality of devices associated with data applications; and

enable logic coupled to each of said plurality of devices and adapted to provide at least one data valid signal that identifies which of said plurality of devices is associated with a particular packet of said time-division multiplexed serial data.

***Swenson and Zaun Fail, In Any Combination, To Teach Or Suggest
The Recited Enable Logic Of Claim 1***

The Office action acknowledges that Swenson fails to teach or suggest enable logic coupled to each of said plurality of devices and adapted to provide at least one data valid signal that identifies which of said plurality of devices is associated with a particular packet of said time-division multiplexed serial data – as is recited by Claim 1. See, e.g., 8/25/2006 Office action, pg.5, ll. 5-8.

In an attempt to remedy this admitted shortcoming of Swenson, the Office action relies upon select teachings of Zaun. More particularly, the Office action argues Zaun discloses logic control block 202 is adapted to provide at least one data valid signal that identifies which of a plurality of packet buffers (packet buffers 1-6) are associated with a particular packet. See, e.g., 8/25/2006 Office action, pg.5, ll. 9-12 (“Zaun et al. discloses, see figure 1, figure 2, enable logic (IP control loci packet validation) adapted to provide at least one data valid signal that identifies which of a plurality of devices (packet buffer #1, #2, #3, #4, #5, #6) are associated with a particular packet.”). Applicant respectfully submits that the Examiner’s reliance is misplaced as Zaun does not teach or suggest the limitations alleged in the Office action.

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A detailed review of Zaun (see Fig. 1) shows six input interfaces 118, PID filter tables 122, and input processors 120. Thus, Zaun can accept six separate MPEG-2 input streams. See, e.g., U.S. Pat. Pub. No. 2002/0024610, par. [0016]. The six input streams can be asynchronous and can have different information rates. See, e.g., U.S. Pat. Pub. No. 2002/0024610, par. [0016]. The input processing section 102 is designed to accept the input streams, drop undesired packets, and store the accepted packet data, an input timestamp, and control information in the packet buffers, where they are presented to the output processor. See, e.g., U.S. Pat. Pub. No. 2002/0024610, par. [0016]. Thus, Fig. 1 of Zaun shows six buffers that work with six input processors, respectively. However, Fig. 1 of Zaun clearly shows that each input processor provides an output to only a corresponding one of the packet buffers – and cannot choose which one it is to use. See, e.g., Fig. 1 (where each output processor feeds only a corresponding one of the buffers).

Fig. 2 of Zaun shows that each input processor includes the control logic 202 relied upon by the Examiner. Thus, because each input processor only feeds a single packet buffer, it is clear that the control logic 202 incorporated within each input processor cannot identify which of packet buffers 1-6 are associated with a particular packet – as they are limited to working with a single packet buffer. See also, Fig. 2 (which includes only a single output to a single packet buffer).

Accordingly, Zaun fails to remedy at least the above discussed deficiency of Swenson, namely, that Swenson fails to teach or suggest enable logic coupled to each of said plurality of devices and adapted to provide at least one data valid signal that identifies which of said plurality of devices is associated with a particular packet of said time-division multiplexed serial data – as is recited by Claim 1.

For purposes of completeness, while Zaun may teach that IP control logic 202 extracts the PID number from the MPEG stream of the input packets in the 8-bit parallel data and sends the PID number to the address

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lines of the PID table 122 (as well as a PID number buffer 203) – this does not equate to identifying which of said plurality of devices is associated with a particular packet of said time-division multiplexed serial data. Rather, if the PID table 122 returns a "valid" bit, either alone or with a "priority" bit if the IP control logic 202 is in a priority mode, the packet will be considered validated and sent to only the single corresponding packet buffer 104 for storage.

***Swenson and Zaun Fail, In Any Combination, To Teach Or Suggest
The Recited Serial-To-Parallel Converter Of Claim 1***

The Final Office action acknowledges that Applicant has pointed out that Swenson fails to teach or suggest providing a packet of said time-division multiplexed serial data in parallel form on a plurality of parallel output lines to one of a plurality of devices associated with data applications – as is recited by Claim 1. *See, e.g., 8/25/2006 Office action, par. 2, ll. 3-5.* The Final Office action argues this is unpersuasive because Swenson shows providing packets to devices 51-58 in Fig. 3. Applicant respectfully disagrees.

As Applicant explained in its prior response mailed February 3, 2006, Fig. 3 of Swenson shows "a parallel-to-serial converter" and not a "serial-to-parallel converter", such as is shown in Fig. 1 of Swenson. Registers 51-58 of the parallel-to-serial converter of Fig. 3 of Swenson are not part of the serial-to-parallel converter of Fig. 1 of Swenson. Instead, registers 51-58 of the parallel-to-serial converter of Fig. 3 of Swenson are loaded one register at a time using parallel received data stored in RAM 40. *See, U.S. Pat. No. 5,926,120, col. 4, ll. 18-30.* Accordingly, the registers 51-58 of the parallel-to-serial converter of Fig. 3 of Swenson cannot and do not in any way suggest that registers 21-28 of the serial-to-parallel converter of Fig. 1 of Swenson have a plurality of parallel output lines for providing thereon a packet of said time-division multiplexed serial data in parallel form to one of a plurality of devices associated with data applications.

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Applicant again directs Examiner's attention to the fact that Swenson shows registers 21-28 for providing serial to parallel output, but says nothing about providing the packet to one of a plurality of devices associated with data applications.

Accordingly, Applicant submits a *prima facie* case of obviousness of Claim 1 is lacking, at least by reason that Swenson and Zaun fail, in any combination, to teach or suggest each of the limitations of Claim 1. Reconsideration and removal of this 35 U.S.C. 103 rejection is requested. Applicant also requests reconsideration and removal of the rejections of Claims 3-5 as well, at least by virtue of these claims' ultimate dependency upon a patentably distinct base Claim 1.

With regard to Claim 6, it analogously recites, *inter alia*, "providing at least one data valid signal that identifies which of said plurality of devices are associated with said outputted packet of parallel data." Accordingly, Applicant submits present Claim 6 patentably distinguishes over the combined teachings of Swenson and Zaun for at least the reasons discussed with regard to Claim 1. Reconsideration and removal of the rejection of Claim 6 is requested. Applicant also requests reconsideration and removal of the rejections of Claims 8 and 9, at least by virtue of these claims' ultimate dependence upon a patentably distinct base Claim 1.

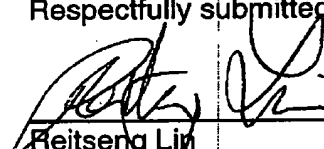
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CONCLUSION

Having fully addressed the Examiner's rejections it is believed that, in view of the preceding amendments and remarks, this application stands in condition for allowance. No fee is believed due in regard to the present amendment. However, if a fee is due, please charge the fee to Deposit Account 07-0832. Accordingly then, reconsideration and allowance are respectfully solicited. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the applicant's attorney at 609-734-6813, so that a mutually convenient date and time for a telephonic interview may be scheduled.

Respectfully submitted,

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